Refine Search

Search Results -

Terms	Documents
L1 same (mode or phase)	25

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L2

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, July 21, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same (mode or phase)	25	L2
L1	bridge same "state machine" same (processor or microprocessor or (micro adj1 processor))	170	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 same (mode or phase)	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Thursday, July 21, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L1 same (mode or phase)	0	L3
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same (mode or phase)	25	L2
L1	bridge same "state machine" same (processor or microprocessor or (micro adj1 processor))	170	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(709/253 |712/32 |710/306 |710/315 |710/100 |710/313 |710/52 |710/305 |710/5 |710/33).ccls.	6948

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Thursday, July 21, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L1	710/306,315,100,313,52,305,5,33;712/32;709/253.ccls.	6948	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L3	33

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

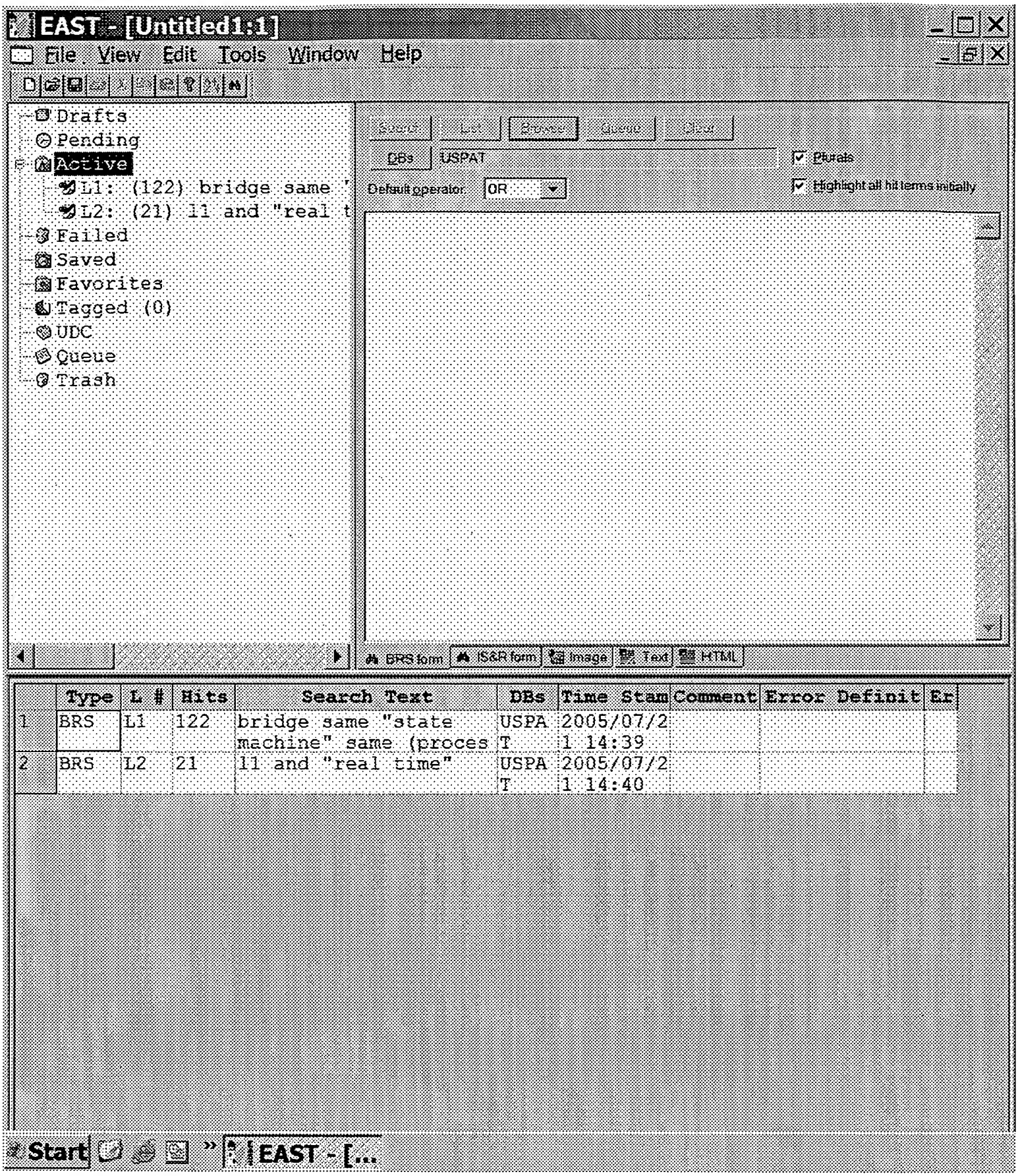
Recall Text | Clear | Interrupt

Search History

DATE: Thursday, July 21, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L4	l1 and L3	33	L4
L3	(bridge same "state machine") and "real time"	182	L3
L2	bridge same "state machine" same "real time"	3	L2
L1	710/306,315,100,313,52,305,5,33;712/32;709/253.ccls.	6948	L1

END OF SEARCH HISTORY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2 BRS L2 21 l1 and "real time" USPA T 2005/07/2 1 14:40
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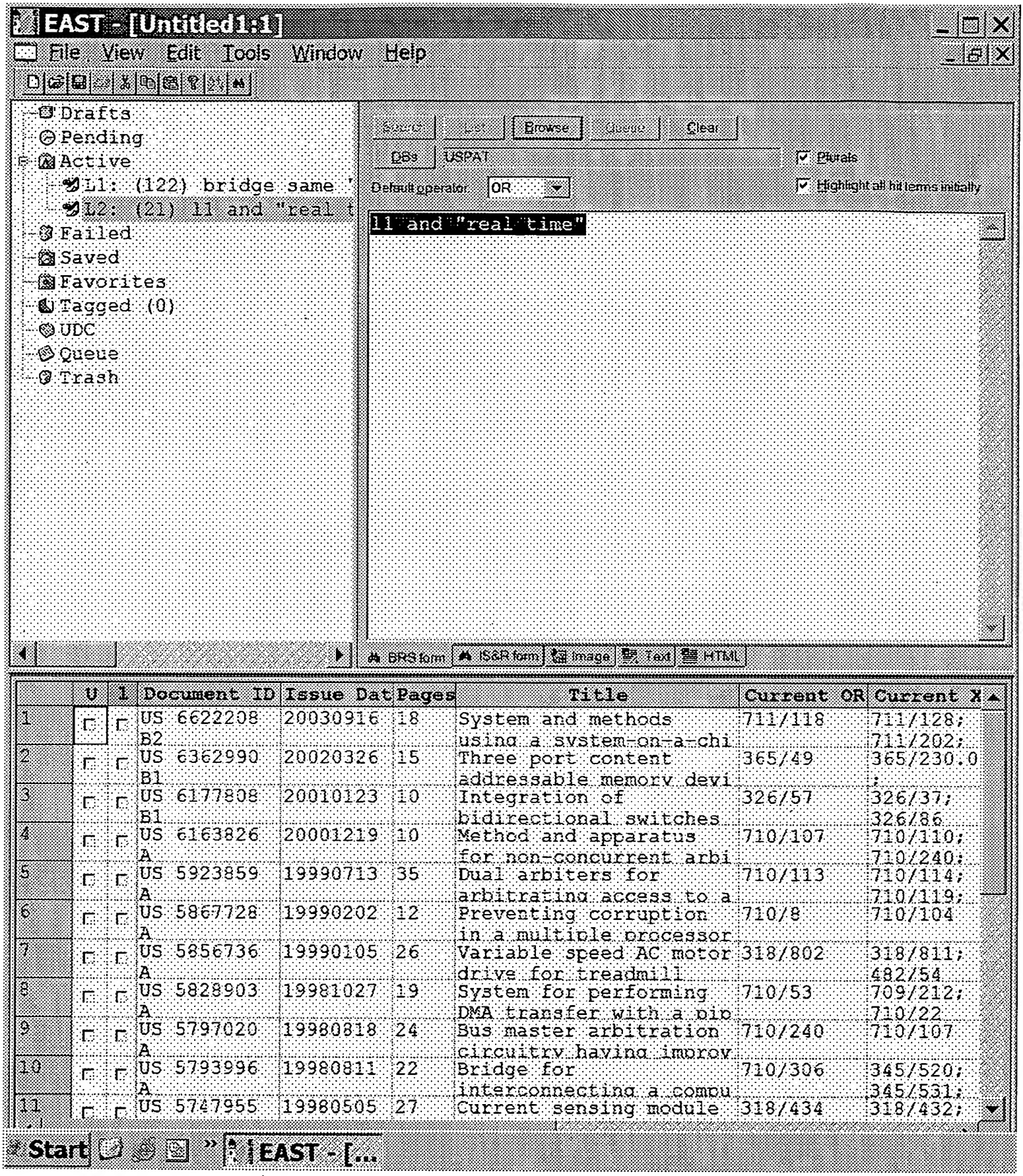
EAST - [Untitled1:1]
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L2: (21) l1 and "real t
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OR
Highlight all hit terms initially
l1 and "real time"
BRS form
IS&R form
Image
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1
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Pages
Title
Current OR
Current X
1 US 6622208 B2 20030916 18 System and methods using a system-on-a-chi 711/118 711/128; 711/202;
2 US 6362990 B1 20020326 15 Three port content addressable memory devi 365/49 365/230.0 ;
3 US 6177808 B1 20010123 10 Integration of bidirectional switches 326/57 326/37; 326/86
4 US 6163826 A 20001219 10 Method and apparatus for non-concurrent arbi 710/107 710/110; 710/240;
5 US 5923859 A 19990713 35 Dual arbiters for arbitrating access to a 710/113 710/114; 710/119;
6 US 5867728 A 19990202 12 Preventing corruption in a multiple processor 710/8 710/104
7 US 5856736 A 19990105 26 Variable speed AC motor drive for treadmill 318/802 318/811; 482/54
8 US 5828903 A 19981027 19 System for performing DMA transfer with a pip 710/53 709/212; 710/22
9 US 5797020 A 19980818 24 Bus master arbitration circuitry having improv 710/240 710/107
10 US 5793996 A 19980811 22 Bridge for interconnecting a compu 710/306 345/520; 345/531;
11 US 5747955 A 19980505 27 Current sensing module 318/434 318/432;
Start
EAST - [...

Results for "(bridge<in>metadata) <and> (state machine<in>metadata)"

e-mail printer friendly

Your search matched 16 of 1194402 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

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New Search

Modify Search

(bridge<in>metadata) <and> (state machine<in>metadata)

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

1. **Bridging the gap between formal specification and analysis of communication protocols**
Miller, R.E.; Yong Xue;
Computers and Communications, 1996., Conference Proceedings of the 1996 IEEE Fifteenth Annual International Phoenix Conference on
27-29 March 1996 Page(s):225 - 231
Digital Object Identifier 10.1109/PCCC.1996.493638
AbstractPlus | Full Text: PDF(664 KB) IEEE CNF

2. **Synchronous protocol automata: a framework for modelling and verification of SoC communication architectures**
D'silva, V.; Ramesh, S.; Sowmya, A.;
Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings
Volume 1, 16-20 Feb. 2004 Page(s):390 - 395 Vol.1
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3. **One-chip solution in 0.35 /spl mu/m standard CMOS for electronic ballasts for fluorescent lamps**
Killat, D.; Schmidt, J.; Baumgaertner, A.; Baraniecki, R.; Salzmann, O.;
System-on-Chip, 2003. Proceedings. International Symposium on
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4. **Distributed computing with the CLAN network**
Riddoch, D.; Mansley, K.; Pope, S.;
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28 Feb.-3 March 1994
Digital Object Identifier 10.1109/EDTC.1994.326908
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6. **Bridging the gap between digital circuits and microprocessors**
Carpinelli, J.D.; Rosenstark, S.;
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Digital Object Identifier 10.1109/13.231513

AbstractPlus | Full Text: PDF(472 KB) IEEE JNL

7. **A framework for testing special-purpose memories**
Sidorowicz, P.R.; Brzozowski, J.A.;
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Digital Object Identifier 10.1109/TCAD.2002.804375
AbstractPlus | References | Full Text: PDF(508 KB) IEEE JNL

8. **Synchronous protocol automata: a framework for modelling and verification of SoC communication architectures**
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Digital Object Identifier 10.1049/ip-cdt:20045097
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9. **Bridge over troubled wrappers:automated interface synthesis**
D'silva, V.; Ramesh, S.; Sowmya, A.;
VLSI Design, 2004. Proceedings. 17th International Conference on
2004 Page(s):189 - 194
Digital Object Identifier 10.1109/ICVD.2004.1260923
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10. **Logician in the land of OS: abstract state machines in Microsoft**
Gurevich, Y.;
Logic in Computer Science, 2001. Proceedings. 16th Annual IEEE Symposium on
16-19 June 2001 Page(s):129 - 136
Digital Object Identifier 10.1109/LICS.2001.932489
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11. **Self test architecture for testing complex memory structures**
Zarrineh, K.; Adams, R.D.; Eckenrode, T.J.; Gregor, S.P.;
Test Conference, 2000. Proceedings. International
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Digital Object Identifier 10.1109/TEST.2000.894248
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12. **Compiling Verilog into timed finite state machines**
Szu-Tsung Cheng; Brayton, R.K.; York, G.; Yelick, K.; Saldanha, A.;
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13. **Active objects: a paradigm for communications and event driven systems**
Caal, G.; Divin, A.; Petitpierre, C.;
Global Telecommunications Conference, 1994. GLOBECOM '94. 'Communications: The Global Bridge'., IEEE
28 Nov.-2 Dec. 1994 Page(s):485 - 489 vol.1
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14. **On testing hierarchies for protocols**
Sidhu, D.P.; Motteler, H.; Vallurupalli, R.;
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Digital Object Identifier 10.1109/90.251917
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15. **Scheduling of transactions for system-level test-case generation**
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16. **SpecTRM: a CAD system for digital automation**
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Volume 1, 31 Oct.-7 Nov. 1998 Page(s):B52/1 - B52/8 vol.1
Digital Object Identifier 10.1109/DASC.1998.741474

AbstractPlus | Full Text: PDF(720 KB) IEEE CNF

Bridging the gap between digital circuits and microprocessors

Carpinelli, J.D. Rosenstark, S.
Dept. of Electr. & Comput. Eng., New Jersey Inst. of Technol., Newark, NJ, USA;

This paper appears in: **Education, IEEE Transactions on**
Publication Date: Aug. 1993
Volume: 36 , Issue: 3
On page(s): 334 - 339
ISSN: 0018-9359
CODEN: IEEDAB
INSPEC Accession Number:4520712
Digital Object Identifier: 10.1109/13.231513
Posted online: 2002-08-06 18:43:53.0

Abstract
Most electrical and computer engineering students understand digital circuits and microprocessors, but fail to appreciate that a microprocessor is just a complex finite state machine. The authors present a three experiment sequence which takes the students from the design of a simple EEPROM-based finite **state machine** through a two-chip microsequencer to a 4-bit central processing unit (CPU)

Index Terms
Inspec

Controlled Indexing
EPROM computer science education digital circuits educational courses finite **state machines** microprocessor chips

Non-controlled Indexing
4-bit central processing unit CPU EEPROM-based finite **state machine** complex finite **state machine** computer engineering students digital circuits electrical engineering students microprocessor design microprocessors two-chip microsequencer

Author Keywords
Not Available

References

No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.

View Search Results | Previous Article | Next Article

L2: Entry 1 of 25 File: PGPB Mar 17, 2005

PGPUB-DOCUMENT-NUMBER: 20050060479
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050060479 A1

TITLE: High speed and flexible control for bridge controllers

PUBLICATION-DATE: March 17, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Deng, Brian Tse	Richardson	TX	US	
Nie, Dinghui Richard	Plano	TX	US	
Erickson, Joseph M.	Frisco	TX	US	

APPL-NO: 10/ 651524 [PALM]
DATE FILED: August 29, 2003

INT-CL: [07] G06 F 13/36

US-CL-PUBLISHED: 710/306
US-CL-CURRENT: 710/306

REPRESENTATIVE-FIGURES: 2

ABSTRACT:

A bridge controller controls the data flow to/from a USB bus to/from an ATA/ATAPI drive, such as an ATA hard drive or ATAPI CD or DVD drive. The bridge controller has a state machine which receives the CBW in a background mode in real time as the packet is being transferred to the bridge controller. The state machine uses the CBW to set up the data transfer. The bridge controller also has a programmable processor which is coupled to the CBW once it is received in a buffer memory. The programmable processor makes changes in the set up of the receiving device for the transfer, if needed, and initiates the data transfer.

L2: Entry 5 of 25 File: PGPB Feb 12, 2004

PGPUB-DOCUMENT-NUMBER: 20040030861
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040030861 A1

TITLE: Customizable computer system

PUBLICATION-DATE: February 12, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Plackle, Bart	Diest		BE	
Herremans, Kurt	Hasselt		BE	

APPL-NO: 10/ 609141 [PALM]
DATE FILED: June 27, 2003

RELATED-US-APPL-DATA:
Application is a non-provisional-of-provisional application 60/392344, filed June 27, 2002,

INT-CL: [07] G06 F 15/00, G06 F 15/76

US-CL-PUBLISHED: 712/32
US-CL-CURRENT: 712/32

REPRESENTATIVE-FIGURES: 2

ABSTRACT:

A customizable computing system, having a microprocessor and a programmable logic device coupled to the microprocessor via a dedicated bus. The programmable logic device includes a configuration to provide I/O functionality to the system and may be a field programmable gate array. The programmable logic device operates as both a north bridge and a south bridge as is understood by those of ordinary skill in the art. Requests are received from the microprocessor in the programmable logic device over the dedicated bus and are processor specific requests. The processor specific requests are translated into processor dependent commands by a bridge. After the processor specific requests are translated into processor dependent commands, the commands are forwarded to processor independent I/O structures which interface with both internal and external peripheral devices to the customizable computing system.

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This U.S. patent application claims priority from provisional patent application Serial No. 60/392,344 filed on Jun. 27, 2002 entitled "Customizable Computer System" and bearing attorney docket 2684/102 which is incorporated herein by reference in its entirety.

L2: Entry 19 of 25 File: USPT Aug 11, 1998

US-PAT-NO: 5793996
DOCUMENT-IDENTIFIER: US 5793996 A

TITLE: Bridge for interconnecting a computer system bus, an expansion bus and a video frame buffer

DATE-ISSUED: August 11, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Childers; Brian A.	Santa Clara	CA		
Baden; Eric A.	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 434196 [PALM]
DATE FILED: May 3, 1995

INT-CL: [06] H01 J 13/00

US-CL-ISSUED: 395/309; 395/306, 395/311, 395/307, 395/287, 395/290, 395/851, 395/858, 395/857, 395/847, 395/509, 395/511, 395/512, 395/520, 395/521, 395/526
US-CL-CURRENT: 710/306; 345/520, 345/531, 345/539, 710/107, 710/110, 710/27, 710/31, 710/37, 710/38

FIELD-OF-SEARCH: 395/289, 395/290, 395/287, 395/306, 395/308, 395/311, 395/307, 395/858, 395/476, 395/850, 395/250, 395/281, 395/284, 395/842, 395/847, 395/504, 395/509, 395/511, 395/512

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4935868	June 1990	Dulac	395/308
☐	5255374	October 1993	Aldereguia et al.	395/308
☐	5257348	October 1993	Roskowski et al.	
☐	5257391	October 1993	Dulac et al.	395/800
☐	5263138	November 1993	Wasserman et al.	
☐	5274753	December 1993	Roskowski et al.	
☐	5301272	April 1994	Atkins	

☐	5359715	October 1994	Heil et al.	395/308
☐	5488695	January 1996	Cutter	395/290
☐	5544334	August 1996	Noll	395/309
☐	5553249	September 1996	Datwyler et al.	395/308
☐	5566306	October 1996	Ishida	395/309
☐	5596729	January 1997	Lester et al.	395/308
☐	5606672	February 1997	Wade	395/308
☐	5611058	March 1997	Moore et al.	395/309
☐	5619728	April 1997	Jones et al.	395/847
☐	5621902	April 1997	Cases et al.	395/309
☐	5634013	May 1997	Childers et al.	395/280
☐	5640545	June 1997	Baden et al.	395/515

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PowerPC 601 RISC Microprocessor User's Manual, pp. 2-42 through 2-70; 8-1 through 8-36; and 9-1 through 9-52, published by Motorola in 1993.
PCI Local Bus Specification, Review Draft Revision 2.1, published Oct. 21, 1994 by the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214.
PCI Multimedia Design Guide, Revision 1.0 (Mar. 29, 1994), which is distributed by the PCI Multimedia Working Group (part of the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214).

ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Phan; Raymond N.

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, LLP

ABSTRACT:

In a computer system an apparatus interconnects a first bus, a second bus and a frame buffer, wherein the first bus and the second bus are of incompatible bus architecture types. For example the first bus may be a loosely coupled bus having split-bus transaction capability, such as the ARBus, and the second bus may be a tightly ordered bus, such as the PCI local bus. The apparatus includes bridge hardware for converting access requests from the first bus into suitable requests for the second bus. Data paths within the apparatus allow data to be routed from one bus to another. The apparatus further includes a frame buffer controller that is accessible from either of the first or second buses for performing read or write operations from/to the frame buffer. Data path logic allows data to be routed from any of the first bus, second bus and frame buffer to any other one of these three locations. In a preferred embodiment, the data paths are fabricated on a first integrated circuit, and all of control logic is fabricated on a second integrated circuit. The partitioning of hardware in this manner allows for an efficient interface to be provided between the two chips.

12 Claims, 12 Drawing figures

Previous Doc Next Doc Go to Doc#

L2: Entry 19 of 25 File: USPT Aug 11, 1998

US-PAT-NO: 5793996
DOCUMENT-IDENTIFIER: US 5793996 A

TITLE: Bridge for interconnecting a computer system bus, an expansion bus and a video frame buffer

DATE-ISSUED: August 11, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Childers; Brian A.	Santa Clara	CA		
Baden; Eric A.	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 434196 [PALM]
DATE FILED: May 3, 1995

INT-CL: [06] H01 J 13/00

US-CL-ISSUED: 395/309; 395/306, 395/311, 395/307, 395/287, 395/290, 395/851, 395/858, 395/857, 395/847, 395/509, 395/511, 395/512, 395/520, 395/521, 395/526
US-CL-CURRENT: 710/306; 345/520, 345/531, 345/539, 710/107, 710/110, 710/27, 710/31, 710/37, 710/38

FIELD-OF-SEARCH: 395/289, 395/290, 395/287, 395/306, 395/308, 395/311, 395/307, 395/858, 395/476, 395/850, 395/250, 395/281, 395/284, 395/842, 395/847, 395/504, 395/509, 395/511, 395/512

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4935868	June 1990	Dulac	395/308
☐	5255374	October 1993	Aldereguia et al.	395/308
☐	5257348	October 1993	Roskowski et al.	
☐	5257391	October 1993	Dulac et al.	395/800
☐	5263138	November 1993	Wasserman et al.	
☐	5274753	December 1993	Roskowski et al.	
☐	5301272	April 1994	Atkins	

☐	5359715	October 1994	Heil et al.	395/308
☐	5488695	January 1996	Cutter	395/290
☐	5544334	August 1996	Noll	395/309
☐	5553249	September 1996	Datwyler et al.	395/308
☐	5566306	October 1996	Ishida	395/309
☐	5596729	January 1997	Lester et al.	395/308
☐	5606672	February 1997	Wade	395/308
☐	5611058	March 1997	Moore et al.	395/309
☐	5619728	April 1997	Jones et al.	395/847
☐	5621902	April 1997	Cases et al.	395/309
☐	5634013	May 1997	Childers et al.	395/280
☐	5640545	June 1997	Baden et al.	395/515

OTHER PUBLICATIONS

PowerPC 601 RISC Microprocessor User's Manual, pp. 2-42 through 2-70; 8-1 through 8-36; and 9-1 through 9-52, published by Motorola in 1993.
PCI Local Bus Specification, Review Draft Revision 2.1, published Oct. 21, 1994 by the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214.
PCI Multimedia Design Guide, Revision 1.0 (Mar. 29, 1994), which is distributed by the PCI Multimedia Working Group (part of the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214).

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ASSISTANT-EXAMINER: Phan; Raymond N.

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, LLP

ABSTRACT:

In a computer system an apparatus interconnects a first bus, a second bus and a frame buffer, wherein the first bus and the second bus are of incompatible bus architecture types. For example the first bus may be a loosely coupled bus having split-bus transaction capability, such as the ARBus, and the second bus may be a tightly ordered bus, such as the PCI local bus. The apparatus includes bridge hardware for converting access requests from the first bus into suitable requests for the second bus. Data paths within the apparatus allow data to be routed from one bus to another. The apparatus further includes a frame buffer controller that is accessible from either of the first or second buses for performing read or write operations from/to the frame buffer. Data path logic allows data to be routed from any of the first bus, second bus and frame buffer to any other one of these three locations. In a preferred embodiment, the data paths are fabricated on a first integrated circuit, and all of control logic is fabricated on a second integrated circuit. The partitioning of hardware in this manner allows for an efficient interface to be provided between the two chips.

12 Claims, 12 Drawing figures

Previous Doc Next Doc Go to Doc#

L2: Entry 19 of 25 File: USPT Aug 11, 1998

US-PAT-NO: 5793996
DOCUMENT-IDENTIFIER: US 5793996 A

TITLE: Bridge for interconnecting a computer system bus, an expansion bus and a video frame buffer

DATE-ISSUED: August 11, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Childers; Brian A.	Santa Clara	CA		
Baden; Eric A.	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 434196 [PALM]
DATE FILED: May 3, 1995

INT-CL: [06] H01 J 13/00

US-CL-ISSUED: 395/309; 395/306, 395/311, 395/307, 395/287, 395/290, 395/851, 395/858, 395/857, 395/847, 395/509, 395/511, 395/512, 395/520, 395/521, 395/526
US-CL-CURRENT: 710/306; 345/520, 345/531, 345/539, 710/107, 710/110, 710/27, 710/31, 710/37, 710/38

FIELD-OF-SEARCH: 395/289, 395/290, 395/287, 395/306, 395/308, 395/311, 395/307, 395/858, 395/476, 395/850, 395/250, 395/281, 395/284, 395/842, 395/847, 395/504, 395/509, 395/511, 395/512

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4935868	June 1990	Dulac	395/308
☐	5255374	October 1993	Aldereguia et al.	395/308
☐	5257348	October 1993	Roskowski et al.	
☐	5257391	October 1993	Dulac et al.	395/800
☐	5263138	November 1993	Wasserman et al.	
☐	5274753	December 1993	Roskowski et al.	
☐	5301272	April 1994	Atkins	

☐	5359715	October 1994	Heil et al.	395/308
☐	5488695	January 1996	Cutter	395/290
☐	5544334	August 1996	Noll	395/309
☐	5553249	September 1996	Datwyler et al.	395/308
☐	5566306	October 1996	Ishida	395/309
☐	5596729	January 1997	Lester et al.	395/308
☐	5606672	February 1997	Wade	395/308
☐	5611058	March 1997	Moore et al.	395/309
☐	5619728	April 1997	Jones et al.	395/847
☐	5621902	April 1997	Cases et al.	395/309
☐	5634013	May 1997	Childers et al.	395/280
☐	5640545	June 1997	Baden et al.	395/515

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PowerPC 601 RISC Microprocessor User's Manual, pp. 2-42 through 2-70; 8-1 through 8-36; and 9-1 through 9-52, published by Motorola in 1993.
PCI Local Bus Specification, Review Draft Revision 2.1, published Oct. 21, 1994 by the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214.
PCI Multimedia Design Guide, Revision 1.0 (Mar. 29, 1994), which is distributed by the PCI Multimedia Working Group (part of the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214).

ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Phan; Raymond N.

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, LLP

ABSTRACT:

In a computer system an apparatus interconnects a first bus, a second bus and a frame buffer, wherein the first bus and the second bus are of incompatible bus architecture types. For example the first bus may be a loosely coupled bus having split-bus transaction capability, such as the ARBus, and the second bus may be a tightly ordered bus, such as the PCI local bus. The apparatus includes bridge hardware for converting access requests from the first bus into suitable requests for the second bus. Data paths within the apparatus allow data to be routed from one bus to another. The apparatus further includes a frame buffer controller that is accessible from either of the first or second buses for performing read or write operations from/to the frame buffer. Data path logic allows data to be routed from any of the first bus, second bus and frame buffer to any other one of these three locations. In a preferred embodiment, the data paths are fabricated on a first integrated circuit, and all of control logic is fabricated on a second integrated circuit. The partitioning of hardware in this manner allows for an efficient interface to be provided between the two chips.

12 Claims, 12 Drawing figures

Previous Doc Next Doc Go to Doc#

L2: Entry 23 of 25 File: USPT Oct 22, 1996

US-PAT-NO: 5568613
DOCUMENT-IDENTIFIER: US 5568613 A

TITLE: Dataframe bridge filter with communication node recordkeeping

DATE-ISSUED: October 22, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Futral; William T.	Hillsboro	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Ungermann-Bass, Inc.	Santa Clara	CA			02

APPL-NO: 07/ 939777 [PALM]
DATE FILED: September 3, 1992

INT-CL: [06] G06 F 13/00, G06 F 13/14, G06 F 12/06

US-CL-ISSUED: 395/200.02; 395/200.11, 395/835, 395/839, 364/246, 364/246.12, 364/246.3
US-CL-CURRENT: 709/249; 710/15, 710/19

FIELD-OF-SEARCH: 395/200, 395/800, 395/325, 395/400, 395/200.02, 395/200.11, 395/835, 395/839, 370/94.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4737953	April 1988	Koch et al.	370/94
☐	4811203	March 1989	Hamstra	364/200
☐	4853921	August 1989	Takeda	369/59
☐	4922503	May 1990	Leone	370/85.13
☐	4926420	May 1990	Shimizu	370/94.1
☐	4967353	October 1990	Brenner et al.	364/200
☐	5125085	June 1992	Phillips	395/400
☐	5136580	August 1992	Videlock et al.	370/60
☐	5245606	September 1993	DeSouza	370/85.13
☐	5321695	June 1994	Faulk, Jr.	370/94.1

ART-UNIT: 237

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Krick; Rehana

ATTY-AGENT-FIRM: Townsend and Townsend and Crew

ABSTRACT:

A dataframe filter is provided a local area network bridge to monitor the dataframes transmitted on one network to determine those dataframes destined to be communicated to another network by the network bridge. The filter receives and examines the destination address of each dataframe communicated on the one filter and, searching through a database maintained by the filter, determine whether the destination address is located on the second network and, if so, signals the bridge to copy the dataframe to the second network.

10 Claims, 6 Drawing figures

Previous Doc Next Doc Go to Doc#

L2: Entry 23 of 25 File: USPT Oct 22, 1996

US-PAT-NO: 5568613
DOCUMENT-IDENTIFIER: US 5568613 A

TITLE: Dataframe bridge filter with communication node recordkeeping

DATE-ISSUED: October 22, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Futral; William T.	Hillsboro	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Ungermann-Bass, Inc.	Santa Clara	CA			02

APPL-NO: 07/ 939777 [PALM]
DATE FILED: September 3, 1992

INT-CL: [06] G06 F 13/00, G06 F 13/14, G06 F 12/06

US-CL-ISSUED: 395/200.02; 395/200.11, 395/835, 395/839, 364/246, 364/246.12, 364/246.3
US-CL-CURRENT: 709/249; 710/15, 710/19

FIELD-OF-SEARCH: 395/200, 395/800, 395/325, 395/400, 395/200.02, 395/200.11, 395/835, 395/839, 370/94.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4737953	April 1988	Koch et al.	370/94
☐	4811203	March 1989	Hamstra	364/200
☐	4853921	August 1989	Takeda	369/59
☐	4922503	May 1990	Leone	370/85.13
☐	4926420	May 1990	Shimizu	370/94.1
☐	4967353	October 1990	Brenner et al.	364/200
☐	5125085	June 1992	Phillips	395/400
☐	5136580	August 1992	Videlock et al.	370/60
☐	5245606	September 1993	DeSouza	370/85.13
☐	5321695	June 1994	Faulk, Jr.	370/94.1

ART-UNIT: 237

PRIMARY-EXAMINER: Lee; Thomas C.

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ATTY-AGENT-FIRM: Townsend and Townsend and Crew

ABSTRACT:

A dataframe filter is provided a local area network bridge to monitor the dataframes transmitted on one network to determine those dataframes destined to be communicated to another network by the network bridge. The filter receives and examines the destination address of each dataframe communicated on the one filter and, searching through a database maintained by the filter, determine whether the destination address is located on the second network and, if so, signals the bridge to copy the dataframe to the second network.

10 Claims, 6 Drawing figures

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US005923859A

United States Patent [19]

Melo et al.

[11] Patent Number: 5,923,859

[45] Date of Patent: Jul. 13, 1999

[54] DUAL ARBITERS FOR ARBITRATING ACCESS TO A FIRST AND SECOND BUS IN A COMPUTER SYSTEM HAVING BUS MASTERS ON EACH BUS

[75] Inventors: Maria L. Melo; Robert Allen Lester, both of Houston, Tex.

[73] Assignee: Compaq Computer Corporation, Houston, Tex.

[21] Appl. No.: 08/974,169

[22] Filed: Nov. 19, 1997

Related U.S. Application Data

[63] Continuation of application No. 08/421,209, Apr. 13, 1995, abandoned.

[51] Int. Cl.[6] G06F 13/00

[52] U.S. Cl. 395/293; 395/294; 395/295; 395/725

[58] Field of Search 395/293, 294, 395/296, 726, 728

[56] References Cited

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5,212,795	5/1993	Allison	395/725
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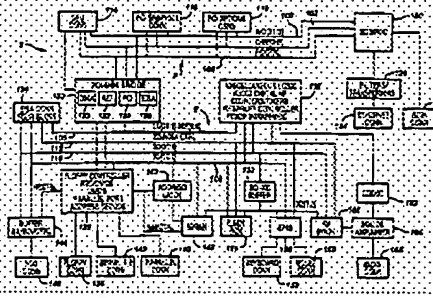
Peripheral Components, Intel Corp., pp. 1-215, 1-222 to 1-225, 1-245 to 1-246, 1-265 to 1-267, 1-280 to 1-285 (1993).

Primary Examiner—Ayaz R. Sheikh
Assistant Examiner—Eric S. Thlang
Attorney, Agent, or Firm—Akin, Gump, Strauss, Hauer & Feld, L.L.P.

[57] ABSTRACT

Arbitration circuitry in a computer system having a plurality of arbiters for arbitrating requests from bus masters on a PCI bus and an EISA bus. Each of the PCI and EISA buses have a plurality of masters. The PCI bus utilizes a modified LRU arbitration scheme, while the EISA bus utilizes a rotating priority scheme. The arbiter on the EISA bus includes a first level of arbitration and a second level of arbitration. The first level is assigned a plurality of requester types to determine the priority between the requestor types. Certain of the first level requestor types include a plurality of devices. If one of those certain requestor types wins priority on the first level arbitration cycle, a second level arbitration is performed to determine the priority between the plurality of devices.

32 Claims, 18 Drawing Sheets



US005793995A

United States Patent [19]

Childers et al.

[11] Patent Number: 5,793,996

[45] Date of Patent: Aug. 11, 1998

[54] BRIDGE FOR INTERCONNECTING A COMPUTER SYSTEM BUS, AN EXPANSION BUS AND A VIDEO FRAME BUFFER

[75] Inventors: Brian A. Childers, Santa Clara; Edir A. Baden, Saratoga, both of Calif.

[73] Assignee: Apple Computer, Inc., Cupertino, Calif.

[21] Appl. No.: 434,196

[22] Filed: May 3, 1995

[51] Int. Cl.[6] H01J 13/00

[52] U.S. Cl. 395/389; 395/306; 395/311; 395/307; 395/287; 395/290; 395/851; 395/858; 395/897; 395/847; 395/509; 395/511; 395/512; 395/520; 395/521; 395/526

[58] Field of Search 395/289, 290, 287, 306, 308, 311, 307, 858, 476, 856, 250, 281, 284, 842, 847, 504, 509, 511, 513, 520, 521, 526

[56] References Cited

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PCI Local Bus Specification, Review Draft Revision 2.1, published Oct. 21, 1994 by the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214.

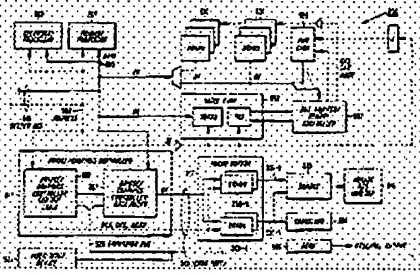
PCI Multimedia Design Guide, Revision 1.0 (May 25, 1994), which is distributed by the PCI Multimedia Working Group (part of the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214).

Primary Examiner—Jack B. Harvey
Assistant Examiner—Raymond N. Phan
Attorney, Agent, or Firm—Burns, Doane, Swecker & Mathis, LLP

[57] ABSTRACT

In a computer system an apparatus interconnects a first bus, a second bus and a frame buffer, wherein the first bus and the second bus are of incompatible bus architecture types. For example the first bus may be a loosely coupled bus having split-bus transaction capability, such as the ARBus, and the second bus may be a tightly ordered bus, such as the PCI local bus. The apparatus includes bridge hardware for converting access requests from the first bus into suitable requests for the second bus. Data paths within the apparatus allow data to be routed from one bus to another. The apparatus further includes a frame buffer controller that is accessible from either of the first or second buses for performing read or write operations from/to the frame buffer. Data path logic allows data to be routed from any of the first bus, second bus and frame buffer to any other one of these three locations. In a preferred embodiment, the data paths are fabricated on a first integrated circuit, and all of control logic is fabricated on a second integrated circuit. The partitioning of hardware in this manner allows for an efficient interface to be provided between the two chips.

11 Claims, 9 Drawing Sheets



L4: Entry 11 of 33 File: USPT Sep 7, 2004

US-PAT-NO: 6789153
DOCUMENT-IDENTIFIER: US 6789153 B1

TITLE: Bridge for coupling digital signal processor to on-chip bus as slave

DATE-ISSUED: September 7, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Stewart; Charles H.	Richardson	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
LSI Logic Corporation	Milpitas	CA			02

APPL-NO: 09/ 847850 [PALM]
DATE FILED: April 30, 2001

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATIONS This application claims priority based on provisional patent application Serial No. 60/270,063, filed Feb. 20, 2001. This application incorporates by reference for all purposes, the following applications, filed on the same date as this application and assigned to the same assignee as the present application: U.S. patent application Ser. No. 09/847,850, filed Apr. 30, 2001, now U.S. Pat. No. 6,687,773, issued Feb. 3, 2004, entitled "Bridge For Coupling Digital Signal Processor to AMBA Bus as Master" by inventors Charles H. Stewart and Keith D. Dang; and U.S. patent application Ser. No. 09/847,848, filed Apr. 30, 2001, entitled "A Parameterizable Queued Memory Access System" by inventor Charles H. Stewart.

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/306; 710/65, 710/311, 710/315
US-CL-CURRENT: 710/306; 710/311, 710/315, 710/65

FIELD-OF-SEARCH: 710/65, 710/306-315

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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☐	6247082	June 2001	Lo et al.	710/105
☐	6467010	October 2002	Pontius et al.	710/305
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☐	6604163	August 2003	Duboc	710/306
☐	6654844	November 2003	Piirainen et al.	710/305
☐	2001/0016885	August 2001	Happonen	710/52

ART-UNIT: 2112

PRIMARY-EXAMINER: Auve; Glenn A.

ASSISTANT-EXAMINER: Patel; Nimesh

ATTY-AGENT-FIRM: Conley, Rose P.C.

ABSTRACT:

A bridge for connecting a DSP to an ASIC on-chip bus as a slave. The bridge couples signals between a DSP internal memory direct memory interface and an on-chip bus such as the AMBA AHB. The bridge includes a generic slave module which provides direct connections to the on-chip bus in the on-chip bus protocol. It also includes a slave engine connected to the DSP memory interface to control read and write transactions with the memory. The generic slave and the slave engine are coupled by a pulse grower and pulse shaver to allow the engine to operate at DSP clock frequency while the generic slave operates at the usually slower on-chip bus frequency. The bridge allows masters in the ASIC to perform read and write transactions with the DSP internal memory.

27 Claims, 12 Drawing figures

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L4: Entry 29 of 33 File: USPT Aug 11, 1998

US-PAT-NO: 5793996
DOCUMENT-IDENTIFIER: US 5793996 A

TITLE: Bridge for interconnecting a computer system bus, an expansion bus and a video frame buffer

DATE-ISSUED: August 11, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Childers; Brian A.	Santa Clara	CA		
Baden; Eric A.	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 434196 [PALM]
DATE FILED: May 3, 1995

INT-CL: [06] H01 J 13/00

US-CL-ISSUED: 395/309; 395/306, 395/311, 395/307, 395/287, 395/290, 395/851, 395/858, 395/857, 395/847, 395/509, 395/511, 395/512, 395/520, 395/521, 395/526
US-CL-CURRENT: 710/306; 345/520, 345/531, 345/539, 710/107, 710/110, 710/27, 710/31, 710/37, 710/38

FIELD-OF-SEARCH: 395/289, 395/290, 395/287, 395/306, 395/308, 395/311, 395/307, 395/858, 395/476, 395/850, 395/250, 395/281, 395/284, 395/842, 395/847, 395/504, 395/509, 395/511, 395/512

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4935868	June 1990	Dulac	395/308
☐	5255374	October 1993	Aldereguia et al.	395/308
☐	5257348	October 1993	Roskowski et al.	
☐	5257391	October 1993	Dulac et al.	395/800
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☐	5359715	October 1994	Heil et al.	395/308
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☐	5566306	October 1996	Ishida	395/309
☐	5596729	January 1997	Lester et al.	395/308
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☐	5611058	March 1997	Moore et al.	395/309
☐	5619728	April 1997	Jones et al.	395/847
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☐	5634013	May 1997	Childers et al.	395/280
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ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Phan; Raymond N.

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, LLP

ABSTRACT:

In a computer system an apparatus interconnects a first bus, a second bus and a frame buffer, wherein the first bus and the second bus are of incompatible bus architecture types. For example the first bus may be a loosely coupled bus having split-bus transaction capability, such as the ARBus, and the second bus may be a tightly ordered bus, such as the PCI local bus. The apparatus includes bridge hardware for converting access requests from the first bus into suitable requests for the second bus. Data paths within the apparatus allow data to be routed from one bus to another. The apparatus further includes a frame buffer controller that is accessible from either of the first or second buses for performing read or write operations from/to the frame buffer. Data path logic allows data to be routed from any of the first bus, second bus and frame buffer to any other one of these three locations. In a preferred embodiment, the data paths are fabricated on a first integrated circuit, and all of control logic is fabricated on a second integrated circuit. The partitioning of hardware in this manner allows for an efficient interface to be provided between the two chips.

12 Claims, 12 Drawing figures

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